L Number	Hits	Search Text	DB	Time stamp
1	0	(retention with lifetime) and (baking or bake) and time and temperature and ferroelectric	EPO; JPO; DERWENT; IBM_TDB	2004/03/06 10:17
2	1	(retention with lifetime) and (baking or bake) and time and temperature and ferroelectric	USPAT; US-PGPUB	2004/03/06 10:24
3	9	(retention with lifetime) and time and temperature and ferroelectric	USPAT; US-PGPUB	2004/03/06 10:26
4	13	(retention with lifetime) and ferroelectric	USPAT; US-PGPUB	2004/03/06 10:26
5	4	((retention with lifetime) and ferroelectric) not ((retention with lifetime) and time and temperature and ferroelectric)	USPAT; US-PGPUB	2004/03/06 10:26

L Number	Hits	Search Text	DB	Time stamp
1	2	(("6238933") or ("6541375")).PN.	USPAT; US-PGPUB	2004/03/05 16:16
2	1	ferroelectric and capacitor and memory and (retention with lifetime with test$3)	USPAT; US-PGPUB	2004/03/05 16:19
3	0	ferroelectric and capacitor and memory and (retention with lifetime with test$3)	EPO; JPO; DERWENT; IBM_TDB	2004/03/05 16:19
4	1	ferroelectric and capacitor and memory and (retention with test$3)	EPO; JPO; DERWENT; IBM_TDB	2004/03/05 16:21
5	0	(ferroelectric and capacitor and memory and (retention with test$3)) and bak$3	EPO; JPO; DERWENT; IBM_TDB	2004/03/05 16:21
6	0	(ferroelectric and capacitor and memory and (retention with test$3)) and temperature	EPO; JPO; DERWENT; IBM_TDB	2004/03/05 16:21
7	41	ferroelectric and capacitor and memory and (retention with test$3)	USPAT; US-PGPUB	2004/03/05 16:21
8	41	(ferroelectric and capacitor and memory and (retention with test$3)) and @ad<20030624	USPAT; US-PGPUB	2004/03/05 17:10
9	26	((ferroelectric and capacitor and memory and (retention with test$3)) and @ad<20030624) and temperature	USPAT; US-PGPUB	2004/03/05 16:22
10	8	(((ferroelectric and capacitor and memory and (retention with test$3)) and @ad<20030624) and temperature) and baking	USPAT; US-PGPUB	2004/03/05 17:09
11	83	retention and (baking or bake) and time and temperature and ferroelectric	USPAT; US-PGPUB	2004/03/05 17:24
12	72	(retention and (baking or bake) and time and temperature and ferroelectric) and state	USPAT; US-PGPUB	2004/03/05 17:10
13	72	((retention and (baking or bake) and time and temperature and ferroelectric) and state) and @ad<20030624	USPAT; US-PGPUB	2004/03/05 17:10
14	43	(((retention and (baking or bake) and time and temperature and ferroelectric) and state) and @ad<20030624) and (test or testing)	USPAT; US-PGPUB	2004/03/05 17:19
15	35	((((retention and (baking or bake) and time and temperature and ferroelectric) and state) and @ad<20030624) and (test or testing)) not ((ferroelectric and capacitor and memory and (retention with test$3)) and @ad<20030624)	USPAT; US-PGPUB	2004/03/05 17:11
16	20	(((retention and (baking or bake) and time and temperature and ferroelectric) and state) and @ad<20030624) and (determine or determining)	USPAT; US-PGPUB	2004/03/05 17:20
17	10	((((retention and (baking or bake) and time and temperature and ferroelectric) and state) and @ad<20030624) and (determine or determining)) not (((((retention and (baking or bake) and time and temperature and ferroelectric) and state) and @ad<20030624) and (test or testing)) not ((ferroelectric and capacitor and memory and (retention with test$3)) and @ad<20030624))	USPAT; US-PGPUB	2004/03/05 17:20
18	0	retention and (baking or bake) and time and temperature and ferroelectric	EPO; JPO; DERWENT; IBM_TDB	2004/03/05 17:24

US-PAT-NO: 6008659

DOCUMENT-IDENTIFIER: US 6008659 A

TITLE: Method of measuring **retention** performance and imprint degradation of ferroelectric films

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Abstract Text - ABTX (1):

A test method for characterizing **retention** performance, both same state and opposite state performance, of ferroelectric capacitors includes the steps of writing an original complementary data state into first and second ferroelectric capacitors after the ferroelectric capacitors have been initialized into an initial valid data state. The first and second ferroelectric capacitors are then subjected to **time and temperature** stress. The original complementary data state from the first and second ferroelectric capacitors is then read, and same state charge (Q.sub.SS) information is collected. An opposite complementary data state is then written in the first and second capacitors. After a short **time** interval, possibly at an elevated **temperature,** the opposite complementary data state from the first and second ferroelectric capacitors is read to gather opposite state charge (Q.sub.OS) information. The original complementary data state is then written into the first and second ferroelectric capacitors. The first and second ferroelectric capacitors are then subjected to further stress cycles, after which the same state and opposite state charge values are recorded. A plot of the same state charge (Q.sub.SS) and opposite state charge (Q.sub.OS)

versus log **time** can be
generated, which has great value for fully characterizing a ferroelectric
capacitor and for predicting the performance of a ferroelectric capacitor in a
memory circuit.

TITLE - TI (1):
Method of measuring **retention** performance and imprint degradation of
ferroelectric films

Parent Case Text - PCTX (1):
This application is related to copending application Ser. No. 08/616,856
filed on the same date as this application entitled "The Use of Calcium and
Strontium Dopants to Improve **Retention** Performance in a PZT Ferroelectric
Film", which is incorporated herein by this reference.

Brief Summary Text - BSTX (2):
This invention relates generally to ferroelectric films and ferroelectric
capacitors. More particularly, the present invention relates to a measurement
method for characterizing the **retention** performance and imprint degradation of
the ferroelectric film, as well as other performance aspects.

Brief Summary Text - BSTX (8):
It is important to note that the peak voltage of the pulse sequence 24 shown
in FIG. 2A is ideally two to three times the "coercive voltage" associated with
the ferroelectric film under test. The "coercive voltage" is shown as points
38 (negative coercive voltage -V.sub.C) and 40 (positive coercive voltage
+V.sub.C) along the x-axis or voltage axis of the hysteresis loop 36 plotted in
FIG. 3. Points 42 and 44 on hysteresis loop 36 define the two stable states of

the ferroelectric film after an externally applied electric field has been removed. Point 42 is generally referred to as an "up" polarization state, and point 44 is generally referred to as a "down" polarization state. These two points 42 and 44 can be arbitrarily defined as a logic one and a logic zero in a one-transistor, one-capacitor ("1T-1C") ferroelectric memory cell, and are compared against a reference level. In a two-transistor, two-capacitor ("2T-2C") ferroelectric memory cell (best seen in FIG. 7), the cell is self-referencing. In this case, the two capacitors are always set in a complementary data state, which means that one capacitor is at point 42 and the other is at point 44. To read the memory, the two capacitors are compared to one another to **determine** which capacitor is polarized up and which capacitor is polarized down. For example, in reference to the capacitors of FIG. 7, a logic one could be defined as capacitor 126 polarized up and capacitor 128 polarized down, in which case a logic zero would be defined as capacitor 126 polarized down and capacitor 128 polarized up.

Brief Summary Text - BSTX (11):

A crucial property of nonvolatile semiconductor memories, and ferroelectric memories in particular is **retention** in the absence of power. **Retention** is the ability to maintain a given data state between the **time** the data state is written and when it is subsequently read. A certain data state is written into a ferroelectric capacitor, or, in the case of a two-transistor, two-capacitor ("2T-2C") memory cell, a complementary data state. After a specified period of **time, and at temperature,** if desired, the data state is read to **determine** whether or not the original data state has been retained in the memory cell.

Retention can be further characterized into an ability to maintain the same state (same state="SS") data or charge (Q.sub.SS) and an ability to read the opposite state data (opposite state="OS") or charge (Q.sub.OS) after maintaining an original data state for an extended period of **time**. Failure to maintain the same data state rarely occurs, and failures are usually related to operation at elevated temperatures near the Curie point in which the ferroelectric material tends to become paraelectric. A small Q.sub.OS charge indicates the failure of a ferroelectric memory cell to read an opposite data state. This failure mechanism is known as "imprint", and is frequently the source of failure in a ferroelectric memory. Imprint is the inability to maintain an opposite data state once an initial data state has been stored under **time and temperature** stress, i.e. the original data state is preferred or has been "imprinted" into the ferroelectric capacitor or film.

Brief Summary Text - BSTX (12):

Prior art techniques for testing **retention in a ferroelectric** film or capacitor included observing the ferroelectric material after a **time and temperature** interval for the presence of a hysteresis loop, single pulse testing, exclusively concentrating on the same state aspect of **retention,** one capacitor tests, and other tests that generally did not emulate the functionality of a ferroelectric capacitor in an actual memory circuit. Further, these tests did not generate graphical predictions for charge loss over **time**.

Brief Summary Text - BSTX (13):

What is desired is a testing technique that can fully